PCIE Bus Quad UARTs and Print Port Chip CH384

Datasheet (II): Quad serial ports + Extend multiple serial ports

Version: 1A

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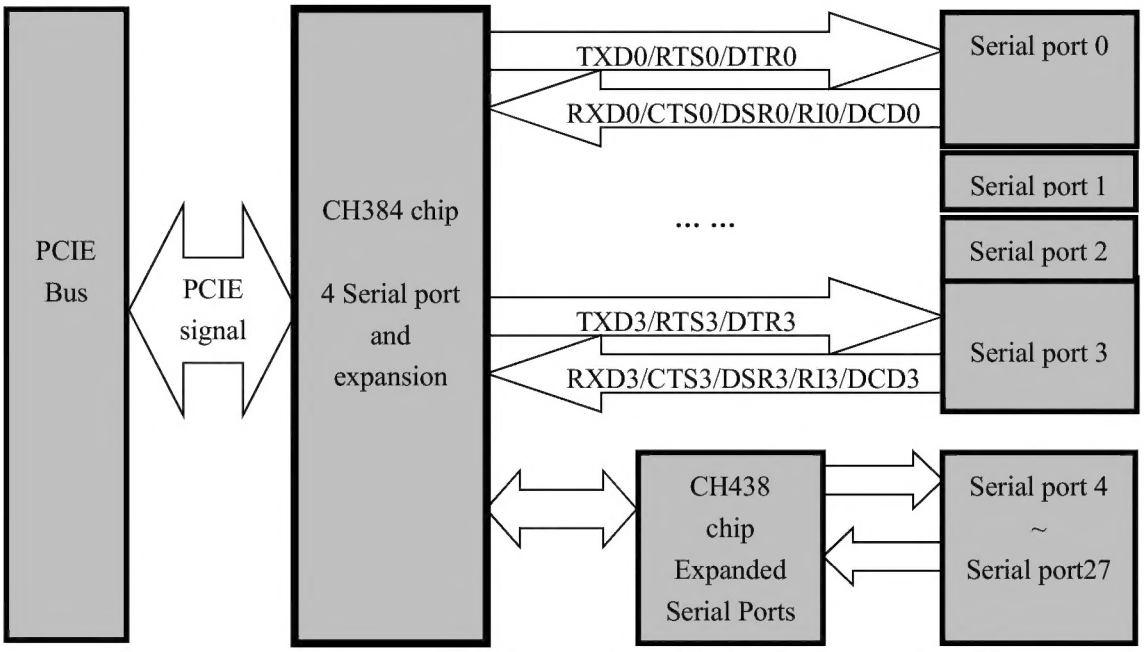
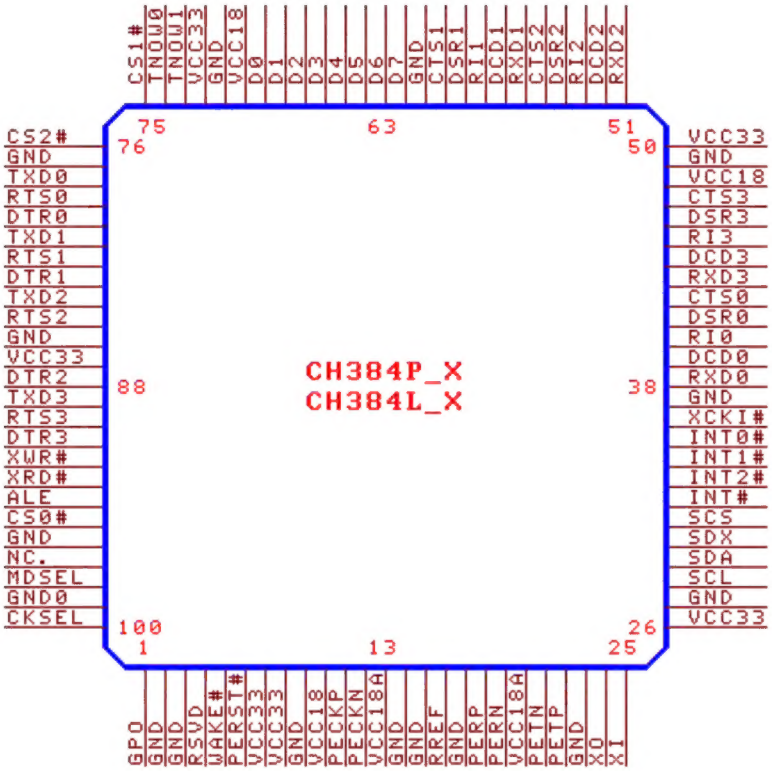
1. Application Block



2. Package

4 Serial port + Parallel port



Please refer to the Datasheet (I) CH384DS1.PDF for application notes and pinout diagrams of the 4 serial ports+ parallel ports.
The CH384P has a built-in 3.3V to 1.8V LDO buck with a single 3.3V supply;
The CH384L requires external supply of both 3.3V and 1.8V.

3. Pin

3.1 Power Line

Pin No.	Pin Name	Type	Pin Description
7,8,26,50,72,87	VCC33	Power	3.3V I/O power
10,48,70	VCC18	Power	1.8V core power
13,20	VCC18A	Power	1.8V transmitting power
97,2,3,9,14,15,17,23,27, 37,49,61,71,77,86,96,99	GND	Power	Common ground
97	NC	Empty pin	Disable connection

3.2 PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
6	PERST#	Input	System reset signal line, active low
11,12	PECKP/PECKN	Input	System reference clock differential input
18,19	PERP/PERN	PCIE input	PCIE receiver differential signal input
22,21	PETP/PETN	PCIE output	PCIE transmitter differential signal output
5	WAKE#	Open-drain output	Bus wake-up output, active at low level, not connected if not used

3.3 Serial Port 0 ~ 3 Signal Line

Pin No.	Pin Name	Type	Pin Description
42/60 55/47	CTS0/CTS1 CTS2/CTS3	Input	MODEM signal, clear to transmit, active low, built-in pull-up resistor
41/59 54/46	DSR0/DSR1 DSR2/DSR3	Input	MODEM signal, data device ready, active low, built-in pull-up resistor
40/58 53/45	RI0/RI1 RI2/RI3	Input	MODEM signal, ringing indication, active low, built-in pull-up resistor
39/57 52/44	DCD0/DCD1 DCD2/DCD3	Input	MODEM signal, carrier detection, active low, built-in pull-up resistor
38/56 51/43	RXD0/RXD1 RXD2/RXD3	Input	Asynchronous serial data input, built-in pull-up resistor
80/83 88/91	DTR0/DTR1 DTR2/DTR3	Output	MODEM signal, data terminal ready, active low
79/82 85/90	RTS0/RTS1 RTS2/RTS3	Output	MODEM signal, request to transmit, active low
78/81 84/89	TXD0/TXD1 TXD2/TXD3	Output	Asynchronous serial data output

74/73	TNOW0/TNOW1	Output	The serial port is transmitting status output (half-duplex transceiver switching), active high

3.4 Extend CH438 signal line

Pin No.	Pin Name	Type	Pin Description
62-69	D7～D0	3-state bidirectional	8-bit parallel data output and input, built-in pull-up, connected to DATA7~DATA0
92	XWR#	Output	Write strobe output, active low, connected to WR#
93	XRD#	Output	Read strobe output, active low, connected to RD#
94	ALE	Output	Address latch enable output of multiplexed address, active high, connected to ALE
95	CS0#	Output	Expanded serial chip select 0 output, connect to CS# of 0# CH438, active low
75	CS1#	Output	Expanded serial chip select 1 output, connect to CS# of 1# CH438, active low
76	CS2#	Output	Expanded serial chip select 2 output, connect to CS# of 2# CH438, active low
35	INT0#	Input	0#CH438 interrupt status input, active low, built-in pull-up resistor
34	INT1#	Input	1#CH438 interrupt status input, active low, built-in pull-up resistor
33	INT2#	Input	2#CH438 interrupt status input, active low, built-in pull-up resistor
32	INT#	Input	Alternate interrupt status input, active low level, built-in pull-up resistor

3.5 Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
16	RREF	Input	System reference current input, requires an external 12KΩ resistor to GND
25	XI	Input	Optional, crystal oscillation input terminal, external crystal and oscillation capacitor
24	XO	Input and output	Optional, inverting output terminal of crystal oscillation, external crystal and oscillation capacitor
28	SCL	Output	General-purpose output, clock output of external configuration chip, can be externally connected to the SCL pin of the serial EEPROM configuration chip 24CXX
29	SDA	Open-drain output and input	General-purpose output and input, built-in pull-up resistor, can be connected to the SDA pin of the serial EEPROM configuration chip 24CXX
30	SDX	3-state bidirectional	General-purpose output and input, built-in pull-up resistor
31	SCS	Output	General-purpose output

100	CKSEL	Input	Serial port clock frequency selection input, built-in pull-up resistor
98	4S1P#	Input	Software recognition mode selection input, built-in pull-up resistor
36	XCKI#	Input	External input serial port clock source selection input, built-in pull-up resistor
1	GPO	Output	General-purpose output
4	RSVD	Reserved	Pins are reserved, disable connection

4. Configuration

The CH384 chip has two main hardware function modes: 4 serial ports + parallel port function mode, and 4 serial ports + extended multi-serial port function mode. The pin definitions in the two functional modes are different. This manual only covers the latter. For the former, please refer to Datasheet (I) CH384DS1.PDF.

The MDSEL pin of the CH384 chip is used to select the software recognition mode:

MDSEL connected to VCC33 or suspended, i.e. MDSEL=1, then it is 8 serial port mode (external 8 serial ports and internal 4 serial ports disabled);

MDSEL connected to GND, i.e. MDSEL=0, it is 28 serial port mode (internal 4 serial ports + external 3*8 serial ports).

The XCKI# pin of the CH384 chip is used to select the clock source of the internal 4 serial ports and disable the internal crystal oscillator in the 28 serial port mode:

XCKI# connected to VCC33 or left floating, that is, XCKI#=1, then the internal crystal oscillator plus the external crystal Or PLL generates a clock;

XCKI# connected to GND, that is, if XCKI#=0, the internal crystal oscillator is disabled and the external clock is input from the XO pin.

The CKSEL pin of the CH384 chip is used to select the clock frequency of the internal 4 serial ports:

CKSEL connected to VCC33 or suspended, i.e. CKSEL=1, the clock is input from the XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient defaults to 1/12 divider, which supports the selection of the 2x frequency again by CK2X or CKnS;

CKSEL connects to GND, i.e. CKSEL=0, then the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is always forced to 2x frequency;

CKSEL connected to PERST# pin, i.e., CKSEL=R, then the internal crystal oscillator is disabled, and the clock is provided by the internal PLL with a frequency of 125MHz, and the internal frequency coefficient is defaulted to 1/68 divider, which supports to select no divider again by CK2X or CKnS.

In 8-port serial mode, CKSEL should be connected to the PERST# pin to disable the internal crystal oscillator, and XCKI# should be left floating. For descriptions of external configuration chips, serial port internal clocks, PCIE configuration space, I/O base address 0 registers, register bit descriptions, and serial port register descriptions, please refer to the Datasheet (I).

5. Function Description

5.1 Query and Interrupt

Multiple serial ports of the CH384 chip share a PCIE interrupt request pin, so after entering the PCIE interrupt service routine, you should first analyze whether the interrupt is requested for CH384 and which serial port the interrupt request is. After entering the interrupt service routine, there are two methods: dedicated status analysis and sequential query:

Dedicated status analysis refers to first reading the IINT internal interrupt status register and the 2 interrupt, the valid IINT bit 3 flag indicates that it is a serial port 3 interrupt, the valid XINT bit 5 flag indicates that it is an external expansion 0#CH438 interrupt, the valid XINT bit 6 flag indicates that it is an external expansion 1#CH438 interrupt, and the valid XINT bit 7 flag indicates that it is an external expansion 1#CH438 interrupt. Expand 2#CH438 interrupt, process and exit directly according to the analysis results, or exit directly if there is no interruption.

Sequential query means to first read the IIR register of serial port 0, process and exit if there is an interrupt, read the IIR register of serial port 1 if there is no interrupt, process and exit if there is an interrupt, read the IIR register of serial port 2 if there is no interrupt, and exit if there is an interrupt. If there is an interrupt, process and exit. If there is no interrupt, read the IIR register of serial port 3. If there is an interrupt, process and exit. If there is no interrupt, read the IIR register of the first serial port. If there is an interrupt, process and exit. If there is no interrupt, process and exit. Get the IIR register of the second externally expanded serial port until the query is completed for all externally expanded serial ports.

After confirming that it is an interrupt of a certain serial port, if necessary, you can further analyze the LSR register to analyze the cause of the interrupt and handle it.

If the serial port works in interrupt mode, you need to set the IER register to allow the corresponding interrupt request, and set OUT2 in the MCR register to allow interrupt output.

If the serial port works in query mode, there is no need to set OUT2 of IER and MCR. You only need to query the LSR register and analyze and process it.

5.2 Serial Port Operation

For specific operations, please refer to the instructions for the single serial port chip 16C550, the dual serial port chip CH432, or the eight serial ports chip CH438.

5.3 Serial Port Operation

For serial port application instructions, please refer to the Datasheet (I).

Note that the output pins of the external expansion serial port through the CH438 chip are all 3.3VLVCMOS levels, compatible with 5VTTL levels, and the input pins are compatible with 3.3VLVCMOS and LVTTL levels, but cannot withstand 5V withstand voltage.

CH384 can be used to expand additional high-speed RS232 serial ports for computers through the PCIE bus, high-baud rate serial ports that support automatic hardware rate control, RS422 or RS485 communication interfaces, SIR infrared communication interfaces, etc.

6. Parameters

Please refer to the Datasheet (I) CH384DS1.PDF

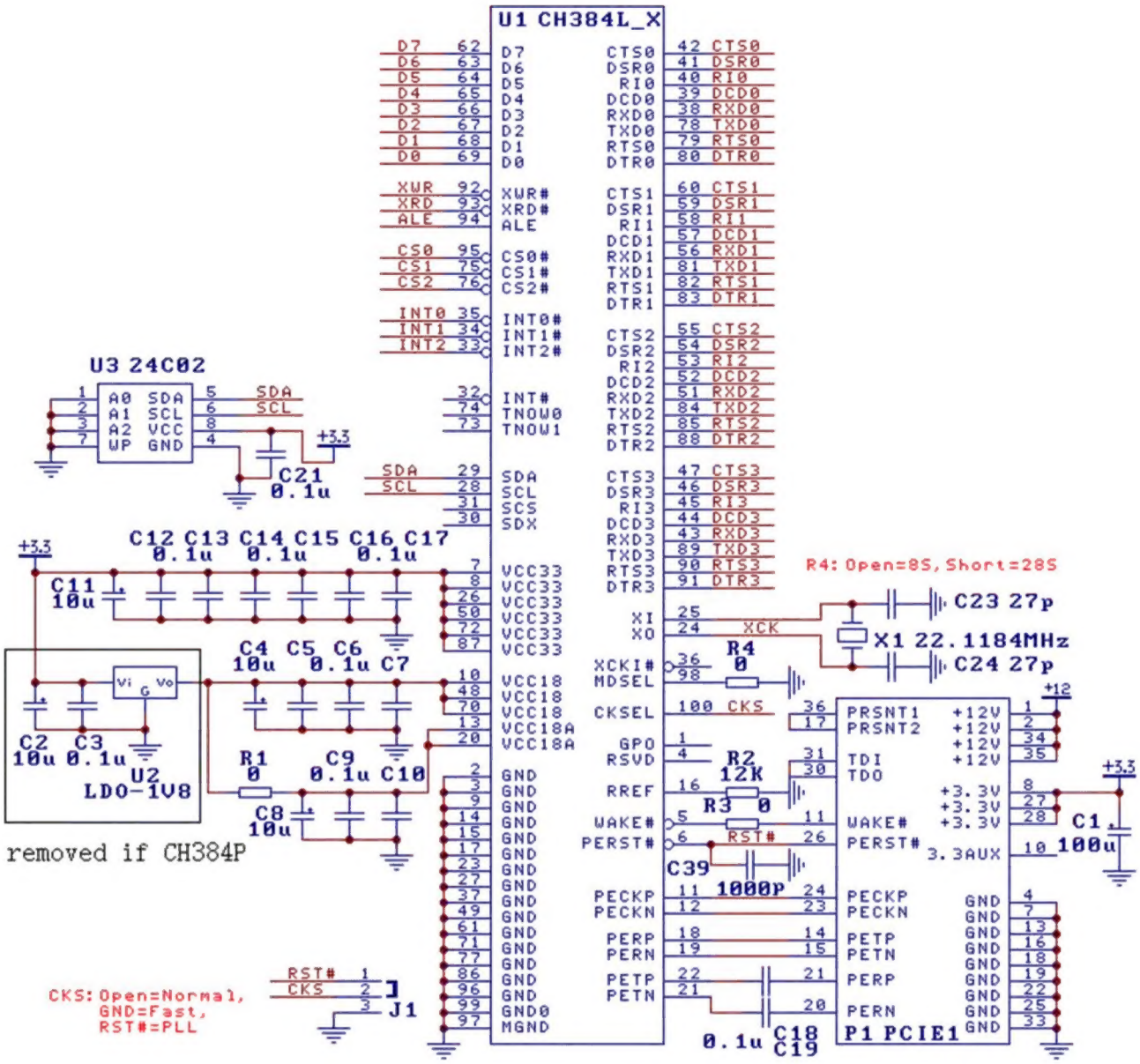
7. Applications

7.1 4 Serial Ports + Parallel Port (Figure Below)

This is the basic circuit of PCIE four serial ports + parallel port/print port based on the CH384 chip. The RS232 level conversion chip is not included in the picture.

U3 is an optional external configuration chip, and the website provides online configuration tool software under Windows system.

Crystal X1 and capacitors C23 and C24 are used in the clock oscillation circuit. Capacitor C39 is used for power-on reset, and other capacitors are used for power supply decoupling. The 10uF capacitor is an MLCC or tantalum capacitor, and the 0.1uF capacitor is a high-frequency capacitor, which are connected in parallel to the power pin of CH384.

For the CH384P chip, the LDO buck is built-in, so U2, C2 and C3 must be removed.

CH384 is a high-frequency circuit. When designing the PCB board, please refer to the PCIE bus specification or the PCIE_PCB.PDF.